IN THE CLAIMS:

1. A method of operating a master/slave system, said method comprising the steps of:

identifying a master receive data phase value to coordinate the transfer of data from a slave device without phase alignment circuitry to a master device with a universal phase aligner;

transferring data from said slave device to said master device in accordance with said master receive data phase value;

characterizing a master transmit data phase value to coordinate the transfer of data from said master device to said slave device; and

routing data from said master device to said slave device in accordance with said master transmit data phase value.

2. The method of claim 1 wherein said identifying step includes the steps of:

applying an alignment signal from said slave device to said master device; and

aligning a receive data clock signal with said alignment signal to obtain said master receive data phase value.

3. The method of claim 2 wherein said identifying step further includes the steps of:

applying a margin offset to said master receive data phase value; and

storing said master receive data phase value.

4. The method of claim 1 wherein said transferring step includes the steps of:

adjusting a system clock signal in accordance with said master receive data phase value to obtain a master receive data clock; and

receiving data at said master device in response to said master receive data clock.

5. The method of claim 1 wherein said characterizing step includes the steps of:

routing request bus data received at said slave device to said master device to form re-routed request bus data; and

aligning a receive data clock signal with said re-routed request bus data to obtain said master transmit data phase value.

6. The method of claim 5 wherein said characterizing step further includes the steps of:

applying a margin offset to said master transmit data phase value; and

storing said master transmit data phase value.

7. The method of claim 1 wherein said aligning step includes the steps of:

adjusting a system clock signal in accordance with said master transmit data phase value to obtain a master transmit data clock; and

transmitting data from said master device in response to said master transmit data clock.

8. A method of operating a master/slave system, said method comprising the steps of:

assessing a phase delay required for synchronized communication between a master device with a universal phase aligner and a slave device without phase alignment circuitry; and

communicating data between said master device and said slave device in accordance with said phase delay.

9. The method of claim 8 wherein said assessing step includes the step of assigning, based upon said phase delay, a first data signal edge that said slave device does not process and a second data signal edge that said slave device does process.

10. The method of claim 8 wherein said assessing step includes the step of assessing a plurality of phase delays required for synchronized communication between said master device and a corresponding plurality of slave devices.

11. The method of claim 10 wherein said communicating step includes the step of identifying a selected phase delay of said plurality of phase delays for communication with a selected slave device of said plurality of slave devices, wherein said communicating step is performed in accordance with said selected phase delay.

12. The method of claim 11 further comprising the step of designating a selected slave device of said plurality of slave devices for communication with said master device.

13. The method of claim 12 wherein said designating step includes the step of applying a control signal to a side band bus linking said plurality of slave devices.

14. The method of claim 12 wherein said designating step includes the step of applying a control signal to a request bus linking said plurality of slave devices.

15. A master/slave system, comprising:

a plurality of slave devices, each slave device including a clock circuit without phase alignment circuitry; and

a master device with a universal phase alignment circuit including a phase value register bank storing a plurality of phase values for said plurality of slave devices, said master device utilizing a selected phase value of said plurality of phase values to alter a system clock signal in accordance with said selected phase value so as to establish synchronous communication between said master device and a selected slave device of said plurality of slave devices.

16. The master/slave system of claim 15 wherein said master device utilizes a first selected phase value to alter said system clock signal to establish a master receive data clock signal to receive data from said selected slave device.

17. The master/slave system of claim 16 wherein said master device utilizes a second selected phase value to alter said system clock signal to establish a master transmit data clock signal to transmit data to said selected slave device.

18. The master/slave system of claim 15 wherein said master device performs a calibration operation in connection with each slave device of said plurality of slave devices to identify said plurality of phase values.

19. The master/slave system of claim 18 wherein said master device adds an offset value to each phase value of said plurality of phase values.

20. In a system comprising a master and at least one slave, the master and at least one slave coupled to a common bus, an auxiliary channel and a common clock, the method of phase aligning an internal clock in the master device and derived from the common clock to enable communication over the data bus with the at least one slave, the method comprising the steps of:

the master causing the at least one slave device to emit a periodic data signal on the data bus by sending a command to the at least one slave device on the auxiliary channel;

the master receiving and sampling the periodic data signal with the internal clock;

the master making a phase adjustment to the internal clock based on the sampled periodic signal to determine a phase boundary of the periodic data signal;

the master storing the value of the phase adjustment in a storage device of the master; and

the master adjusting the phase of the internal clock by the stored phase adjustment value plus an offset to receive data substantially without error from the at least one slave device.

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